In the Abstract:

Please amend the abstract as follows:

An integrated circuit arrangement that has an integrated test structure is provided. The integrated circuit arrangement includes a transistor array having ~~which has~~ vertical FET selection transistors [[and]] electrically coupled to storage capacitors ~~in each case of a transistor array and~~ of an assigned memory cell array, ~~said~~ the storage capacitors being formed vertically into the depth of a substrate in deep ~~trenches~~ trenches. [[a]] The test structure ~~is integrated, which enables~~ may enable a plurality of vertical FET selection transistors ~~with one another~~ by a conductive electrode material embedded in an extended deep ~~trench~~trench. With a test structure of this type, it is possible to evaluate characteristic values for leakage currents and capacitances at different semiconductor junctions and also between different sections of the integrated circuit arrangement and also to perform reliability stress tests.